What is claimed is:

1. A symbol timing synchronizer for generating a timing signal from a sampled input signal being a received input signal sampled at a rate of the timing signal, the received input signal being a continuous phase modulated signal modulated by a symbol sequence generated from a precoded data sequence of an input data sequence, sampled input signal having a sampled inphase component and a sampled quadrature component, the symbol timing synchronizer comprising,

an inphase isolator and a quadrature isolator for respectively isolating the sampled inphase component and sampled quadrature component of the sampled input signal for respectively providing an inphase signal and a quadrature signal,

an inphase serial data demodulator and a quadrature serial data demodulator for respectively receiving and filtering the inphase signal and the quadrature signal for generating an odd filter response and an even filter response, and for converting and sampling the odd and even filter responses into odd data and even data, the odd data and the even data alternately forming an estimate of the input data sequence,

an inphase error magnitude generator and a quadrature error magnitude generator for receiving and filtering the inphase signal and the quadrature signal, for respectively generating and sampling an inphase error magnitude signal and quadrature error magnitude signal for respectively generating a sampled inphase error magnitude signal and a sampled quadrature error magnitude signal,

an inphase mixer and a quadrature mixer for respectively mixing the sampled inphase error magnitude signal with the odd data into an odd error signal, and mixing the quadrature error magnitude signal with the even data for generating an even error signal, the odd data representing an odd sign of the inphase magnitude error signal, the even data representing an even sign of the quadrature magnitude signal, and

an oscillator means for generating the timing signal from the even error signal and the odd error signal, the timing signal for controlling the sampling of the inphase serial data demodulator and the quadrature serial data demodulator and for controlling the sampling of inphase error magnitude generator and a quadrature error magnitude generator for generating the timing signal at a rate of the symbol sequence.

2. The symbol timing synchronizer of claim 1 wherein the oscillator means comprises,

a loop filter for receiving the odd error signal and the even error signal for providing a filter error signal,

a controlled oscillator for receiving the filter error signal for generating the timing signal, and

a modulo counter for providing an odd timing signal for sampling the inphase magnitude error signal, and for providing an even timing signal for sampling the quadrature magnitude error signal.

3. The symbol timing synchronizer of claim 1 wherein,

the inphase magnitude error generator generates the inphase magnitude error signal from a difference between a filter response of the inphase signal and an odd modulo count of the timing signal, the inphase magnitude error generator serving to cross correlate a principal Laurent component of the inphase signal with a gate function relative to the odd modulo count of the timing signal, and

the quadrature magnitude error generator generates the quadrature magnitude error signal from a difference between a filter response of the quadrature signal and an even modulo count of the timing signal, the quadrature magnitude error generator serving to cross correlate a principal Laurent component of the inphase signal with a gate function relative to the even modulo count of the timing signal.

4. The symbol timing synchronizer for claim 1 wherein,

inphase and quadrature serial demodulators respectively filter principal Laurent components of the inphase and quadrature signals for providing odd and even Laurent filter responses, and

inphase and quadrature serial demodulators respectively sample the odd and even Laurent filter responses for generating the odd and even data.

5. The symbol timing synchronizer of claim 1 further comprising

an input sampler for sampling the received signal into the sampled input signal sampled at a rate of the timing signal.

6. The symbol timing synchronizer of the claim 1 further comprising,

a multiplexer for multiplexing the odd and even data into the estimate of the input data sequence.

7. the symbol timing synchronizer of claim 1 wherein,

the received input system is a Gaussian minimum shift keying signal have a bit bandwidth product of 1/5 and a modulation index of 1/2.

8. The symbol timing synchronizer of claim 3 wherein,

the odd modulo count is (2k+1)N where N is the modulo count of the modulo counter, and

the even modulo count is (2k)N where N is the modulo count of the modulo counter

9. The symbol timing synchronizer of claim 1 wherein

the odd error signal is an e_{2k+1} odd error signal, and

the even error signal is an e_{2k} even error signal.

10. The symbol timing synchronizer of claim 1 further comprising

a carrier phase synchronizer for generating a phase adjustment signal from a sampled phase adjusted input signal and the timing signal,

an input mixer for adjusting the received input signal into a phase adjusted input signal, and

an input sampler for sampling the phase adjusted input signal into the sampled phase adjusted input signal.

11. The symbol timing synchronizer of claim 10 wherein the carrier phase synchronizer comprises,

an inphase isolator and a quadrature isolator for respectively isolating the sampled inphase component and sampled quadrature component for providing an inphase signal and a quadrature signal,

an inphase serial data demodulator and a quadrature serial data demodulator for respectively receiving and filtering the inphase signal and the quadrature signal for generating an odd filter response and an even filter response, and for converting and sampling the odd and even filter responses into odd data and even data, the odd data and the even data alternately forming an estimate of the input data sequence,

an odd mixer and an even mixer for respectively mixing the even filter response and the odd data signal into an odd error signal and mixing the odd filter response signal and the even data signal into an even error signal, and

an oscillator means for converting the odd and even error signals into the phase adjustment signal.

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12. A symbol timing synchronizer for generating a timing signal from a sampled input signal being a received input signal sampled at a rate of the timing signal, the received input signal being a continuous phase modulated signal modulated by a symbol sequence generated from a precoded data sequence of an input data sequence, sampled input signal having a sampled inphase component and a sampled quadrature component, the symbol timing synchronizer comprising,

an inphase isolator and a quadrature isolator for respectively isolating the sampled inphase component and sampled quadrature component of the sampled input signal for respectively providing an inphase signal and a quadrature signal,

an inphase early-late gate and a quadrature early-late gate for respectively filtering the inphase signal and the quadrature signal for generating an inphase gate signal and a quadrature gate signal, the inphase and quadrature early-late gates respectively serving to cross correlate the inphase and quadrature signals with gate functions in synchronism with the timing signal,

an inphase transformer and a quadrature transformer for respectively transforming the inphase signal and the quadrature signal for generating an inphase transformed signal and a quadrature transformed signal,

an inphase gate sampler and a quadrature gate sampler for respectively sampling inphase gate signal and the quadrature gate signal for generating a sampled inphase gate signal and a sampled quadrature gate signal,

an inphase transformer sampler and a quadrature transformer sampler for respectively sampling the inphase transformed signal and the quadrature transformed signal for generating a sampled inphase transformed signal and a sampled quadrature transformed signal,

an inphase hard limiter and a quadrature hard limiter for respectively converting the sampled inphase transformed signal into odd data and the sampled quadrature transformed signal into even data,

an inphase mixer and a quadrature mixer for respectively mixing the sampled inphase gate signal and odd data into an odd error signal and mixing the sampled quadrature gate signal and even data signal into an even error signal, and

an oscillator means for generating the timing signal from the even error signal and the odd error signal, the oscillator means for controlling the sampling of the inphase and quadrature gate samplers and the inphase and quadrature transformer samplers for generating the timing signal at a rate of the symbol sequence.

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13. The symbol timing synchronizer of claim 12 wherein the oscillator means comprises,

a loop filter for receiving the odd error signal and the even error signal for providing a filter error signal,

a controlled oscillator for receiving the filter error signal for generating the timing signal, and

a modulo counter for providing an odd timing signal for sampling the inphase magnitude error signal, and for providing an even timing signal for sampling the quadrature magnitude error signal.

14. The symbol timing synchronizer of claim 12 wherein,

the inphase and quadrature early-late gates function as cross correlators for cross correlating a filter response isolating principal Laurent components of the inphase and quadrature signals with a gating function,

the inphase gate signal is an inphase magnitude error signal from the correlation of an inphase early-late gate filter response of the inphase signal and the gating function that is in synchronism with an odd modulo count of the timing signal, and

the quadrature gate signal is a quadrature magnitude error signal from the correlation of a quadrature early-late gate filter response of the quadrature signal and the gating function that is in synchronism an even modulo count of the timing signal.

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15. The symbol timing synchronizer for claim 12 wherein,

the inphase and quadrature transformers, transformer samplers and hard-limiters respectively are inphase and quadrature serial demodulators,

the inphase and quadrature transformer are principal Laurent component filters providing the inphase and quadrature transformed signals that respectively are odd and even Laurent filter responses, and

the odd and even data alternately forming an estimate of the input data sequence.

16. The symbol timing synchronizer of claim 12 further comprising

an input sampler for sampling the received signal into the sampled input signal sampled at a rate of the timing signal, and

a multiplexer for multiplexing the odd and even data into the estimate of the input data sequence.

17. The symbol timing synchronizer of claim 12 wherein,

the received input system is a Gaussian minimum shift keying signal have a bit bandwidth product of 1/5 and a modulation index of 1/2,

the odd modulo count is (2k+1)N where N is the modulo count of the modulo counter,

the even modulo count is (2k)N where N is the modulo count of the modulo counter,

the odd error signal is an e_{2k+1} odd error signal, and

the even error signal is an e_{2k} even error signal.

18. The symbol timing synchronizer of claim 12 further comprising

a carrier phase synchronizer for generating a phase adjustment signal from a sampled phase adjusted input signal and the timing signal,

an input mixer for adjusting the received input signal into a phase adjusted input signal, and

an input sampler for sampling the phase adjusted input signal into the sampled phase adjusted input signal.

19. The symbol timing synchronizer of claim 18 wherein the carrier phase synchronizer comprises,

a carrier inphase isolator and a carrier quadrature isolator for respectively isolating the carrier sampled inphase component and carrier sampled quadrature component for providing a carrier inphase signal and a carrier quadrature signal,

an inphase sampler and a quadrature sampler for respectively sampling at the rate of the timing signal the carrier inphase signal and the carrier quadrature signal for providing a carrier sampled inphase signal and a carrier sampled quadrature signal,

a carrier inphase transformer and a carrier quadrature transformer for respectively transforming the carrier sampled inphase signal and carrier sampled quadrature signal into a carrier inphase transformed signal and a carrier quadrature transformed signal,

a carrier inphase hard limiter and a carrier quadrature hard limiter for respectively converting the carrier inphase transformed signal and carrier quadrature transformed signal into a carrier odd hard limited signal and a carrier even hard limited signal,

a carrier modulo counter for receiving the timing signal and generating a carrier odd timing signal and a carrier even timing signal,

a carrier odd sampler and a carrier even sampler for respectively sampling at the rate of the carrier odd and even timing signals for sampling the carrier odd and even hard limited signals into carrier odd data and carrier even data,

a carrier odd mixer and a carrier even mixer for respecting mixing the carrier quadrature transformed signal and the carrier odd data signal into a carrier odd error signal and the carrier inphase transformed signal and the carrier even data signal into a carrier even error signal, and

a carrier oscillator for converting the carrier odd and even error signals into the phase adjustment signal.

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